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20350 7590 02/27/2009 TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834				
EXAMINER				
LEE, CHUN KUAN				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/749,910

Applicant(s)

DHANOA, KULWINDER

Examiner

Chun-Kuan Lee

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,5-8 and 11-13 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1,2,5-8 and 11-13 is/are rejected.
7) ☒ Claim(s) 1,2,7,8,11 and 13 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 24 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. In view of the Appeal Brief filed on December 04, 2008, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Therefore the FINALITY of the office action dated May 21, 2008 is hereby withdrawn. Currently, claims 3-4, 9-10 and 14-17 are canceled and claims 1-2, 5-8 and 11-13 are pending for examination.

2. The instant application having Application Number: 10/749,910 filed on 12/30/2003 currently has a total of 9 claims pending for examination; there are 3 independent claims and 6 dependent claims, all of which are examined below.

RESPONSE TO ARGUMENTS

3. Applicant's arguments with respect to claims 1-2, 5-8 and 11-13 have been considered but are moot in view of the new ground(s) of rejection.

I. OATH / DECLARATION

4. The oath/declaration has been reviewed by the examiner and is found to comply with the provisions of 37 CFR 1.63.

II. DRAWINGS

5. The drawing(s) have been reviewed by the examiner and are found comply with the provisions of 37 CFR 1.81 to 1.85.

III. SPECIFICATION

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. The disclosure is objected to because of the following informalities:
on page 9, first paragraph (in line 4), element 64 is referred to as the "third buffer;" the examiner suggests correcting the Specification to reflect that the element 64 is the "nth buffer";

on page 11, 1st paragraph (in line 1), "Figure 2 shows" should be corrected to be "Figure 5 shows" as the corresponding elements in the same paragraph are all referring to elements in Figure 5;

on page 11, 4th paragraph (in line 27), the control logic is incorrectly referenced to element 556 of Fig. 5; the examiner suggest correcting the Specification to reflect the control logic of Figure 5 should be element 554;

multiple instances in the Specification reference the control logic of Figure 2 to be element 56; the examiner suggests correcting the Specification to reflect the control logic of Figure 2 should be element 54; and

multiple instances in the Specification refer to the abbreviation of "AHB" without clearly indicating what the abbreviation stands for; the examiner suggests the following amendments to the Specification to clarify the above abbreviation: AHB (Advanced High-performance Bus).

Please note that the request for the replacements as stated above is for the purpose to improve the clarity of the Specification. Appropriate correction is required.

IV. OBJECTIONS TO THE CLAIMS

8. Claims 1-2, 7-8, 11 and 13 are objected to because of the following informalities:

in claim 1, lines 7-8, "... the data burst stored in the corresponding buffer ..." should be replaced with "... the data burst stored in one of the corresponding plurality of buffers ...-;

in claim 1, line 18, "... data for the memory access request being stored ..." should be replaced with "... data for the wrapping memory access request being stored ...-";

in claim 1, line 20, "... and end data in a single buffer avoiding the need ..." should be replaced with "... and end data in the single respective buffer avoiding the need ...-";

in claim 1, line 22, "... in the respective sub-buffer until ..." should be replaced with "... in one of the respective sub-buffers until ...-";

in claim 1, lines 25-26, "... of the single buffer storing the end data ... the indicated sub-buffer to retrieve ..." should be replaced with "... of the single respective buffer storing the end data ... the indicated first sub-buffer to retrieve ...-";

in claim 2, lines 4-5, "... part of the single buffer, then data ... from a second part of the single buffer ..." should be replaced with "... part of the respective buffer, then data ... from a second part of the respective buffer ...-";

in claim 7, line 7, "... assigning each data burst to a respective buffer in a plurality of buffers ..." should be replaced with "... assigning each of said multiple data bursts to a respective buffer in the plurality of buffers ...-";

in claim 7, line 10, "... the data burst stored in the corresponding buffer ..." should be replaced with "... the data burst stored in one of the corresponding plurality of buffers ...-";

in claim 7, lines 16-17, "... and end data in a single buffer avoiding the need ..." should be replaced with "... and end data in the single respective buffer avoiding the need ...-;

in claim 7, lines 18-19, "... in the respective sub-buffer until ..." should be replaced with "... in one of the respective sub-buffers until ...-;

in claim 7, lines 20-22, "... of the single buffer storing the end data ... the indicated sub-buffer to retrieve ..." should be replaced with "... of the single respective buffer storing the end data ... the indicated first sub-buffer to retrieve ...-;

in claim 8, lines 4-5, "... part of single buffer, then reading ... from a second part of the single buffer ..." should be replaced with "... part of the respective buffer, then reading ... from a second part of the respective buffer ...-;

in claim 11, lines 3-4, "... assigning each of said data bursts to a respective ..." should be replaced with "... assigning each of said memory bursts to a respective ...-;

in claim 13, lines 10-11, "... the data burst stored in the corresponding buffer ..." should be replaced with "... the data burst stored in one of the corresponding plurality of buffers ...-;

in claim 13, line 21, "... data for the memory access request being stored ..." should be replaced with "... data for the wrapping memory access request being stored ...-;

in claim 13, lines 22-23, "... and end data in a single buffer avoiding the need ..." should be replaced with "... and end data in the single respective buffer avoiding the need ...-;

in claim 13, line 24, "... in the respective sub-buffer until ..." should be replaced with "... in one of the respective sub-buffers until ...-; and

in claim 13, lines 27-28, "... of the single buffer storing the end data ... the indicated sub-buffer to retrieve ..." should be replaced with "... of the single respective buffer storing the end data ... the indicated first sub-buffer to retrieve ...-.

Please note that the request for the replacements as stated above is for the purpose to improve the clarity of the claim language. Appropriate correction is required.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-2, 7-8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Abramson et al. (US Patent 6,499,077), lizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326).
10. As per claims 1, 7 and 13, Gray teaches a memory controller system, method and programmable logical device, comprising:

at least one bus interface (e.g. devices interface 250 of Fig. 2-3), each bus interface being for connection to at least one respective device (formed within the programmable logic device) (e.g. equivalent to device 221-224 of Fig. 3) for receiving memory access requests (col. 5, l. 19 to col. 8, l. 63);

a memory interface (Fig. 2-3, ref. 200, 270), for connection to a (external) memory device (Fig. 1, ref. 25 and Fig. 2-3, ref. 210) over a memory bus (Fig. 2-3; Fig. 5-6; col. 5, l. 19 to col. 8, l. 63 and col. 9, ll.13-22), wherein the memory interface utilize a list structure to provide the scheduling of data storing in response to the memory access request;

a plurality of buffers (Fig. 3, ref. 202-209) in the memory interface (Fig. 3, ref. 200, 270);

control logic (DMA engine 200 of Fig. 2), for placing received memory access requests (Fig. 6, ref. 307, 308) into a queue of memory access requests (col. 10, l. 65 to col. 11, l. 24), wherein the queue of memory access requests comprising the critical request queue and the non-critical request queue for receiving the respective memory access request,

wherein, in response to receiving memory access requests (Fig. 6, ref. 307, 308) requiring multiple data bursts (Fig. 6, ref. 301-306) (e.g. burst of data for channel 0-2 for devices 221 and 222 of Fig. 6) over the memory bus, each of said multiple data bursts is assigned by the control logic (DMA engine 200 of Fig. 2) to a respective buffer (Fig. 3, ref. 202-209) of the plurality of buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in the respective buffer (col.

2, ll. 47-56; col. 5, l. 19 to col. 8, l. 63 and col. 11, l. 59 to col. 12, l. 6), wherein data for the first device (Fig. 3, ref. 221) may be stored in the first device buffer (Fig. 3, ref. 204), data for the second device (Fig. 3, ref. 222) is stored in the second device buffer (Fig. 3, ref. 206) and so on; and as the memory interface's DMA engine regulate the transferring of data by being responsible for providing data to each device, for monitoring the remaining data in the corresponding device buffers, and for provide arbitration functionality to the devices as well as the memory, it would have been obvious for the DMA engine to implementing the assignments; and

transferring of data in response to the memory access requests (col. 7, ll. 6-42).

Gray does not expressly teach the memory controller system, method and programmable logical device, comprising: each of the plurality of buffers being sized to store a data burst for a memory access request ... ; a single memory access request for the multiple data bursts; wherein, for a wrapping memory access request requiring multiple buffers ... , and wherein the control logic records a value of a pointer

Abramson teaches a system and a method comprising a single memory access request for multiple data bursts by combining multiple requests from multiple peripheral devices (Fig. 5; col. 3, l. 59 to col. 5, l. 38 and col. 8, l. 33 to col. 9, l. 53), by combining with Gray's multiple data bursts for the multiple requests from the multiple devices, the resulting combination further teaches that several requests from the multiple peripheral devices are combined into a single packet of request to be forwarded.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Abramson's single request configuration into Gray's memory controller system for the benefit of having a more cost efficient request interface device by utilizing only a single interface device for multiple requesters (Abramson, col. 9, ll. 50-53) to obtain the invention as specified in claims 1, 7 and 13.

Gray and Abramson do not expressly teach the memory controller system, method and programmable logical device, comprising: each of the plurality of buffers being sized to store a data burst for a memory access request ... ; wherein, for a wrapping memory access request requiring multiple buffers ... , and wherein the control logic records a value of a pointer

Iizuka teaches a buffer system and method comprising:

a plurality of buffers (Fig. 8, ref. 9-1 to 9-3), wherein each of the plurality of buffers sized to store a data burst for a request, each of the plurality of buffers further include a plurality of sub-buffers each sized to store a data beat of the data burst stored in the one of the corresponding plurality of buffers (Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57 and col. 26, ll. 4-39), wherein each FIFO buffer includes the corresponding plurality of sub-buffers for storing the data beat;

a wrapping memory access request requiring multiple buffers (e.g. by combining with Gray and Abramson's single request configuration, the resulting combination teaches the single wrapping memory access request requiring multiple buffers for the multiple requests), data required for each of a beginning and an end of the wrapping

memory access request are assigned to respective sub-buffers of a single respective buffer (e.g. single respective buffer of 9-1, 9-2 or 9-3 of Fig. 8, as the begin and end of data transferring located at the single respective buffer), the beginning and end data for the memory access request being stored concurrently (e.g. concurrently via the cyclical usage of the buffers) from a single data burst in the respective sub-buffers of the single respective buffer, the storing of the beginning and end data in the single respective buffer (e.g. single respective buffer of 9-1, 9-2 or 9-3 of Fig. 8, as the begin and end of data transferring located at the single respective buffer) avoiding the need for an additional data burst to obtain the end data, the data required for the end of the wrapping memory access request being cached in one of the respective sub-buffers until needed for transferring (Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57 and col. 26, ll. 4-39), such as commence utilizing buffer 9-1, then goes to the buffer 9-2 and buffer 9-3, and finally ends at buffer 9-1, and

wherein a first sub-buffer of the single respective buffer (e.g. respective single cyclical FIFO ring buffer 9-1, 9-2 or 9-3 of Fig. 8) storing the end data, such that enabling the returning to the indicated first sub-buffer to retrieve the end data from the single respective buffer (e.g. single cyclical FIFO ring buffer 9-1, 9-2 or 9-3 of Fig. 8) (Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57 and col. 26, ll. 4-39), such as start utilizing buffer 9-1, buffer 9-2, buffer 9-3, and ends utilizing buffer 9-1.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include lizuka's buffering architecture into Gray and Abramson's device buffers for the benefit of implementing a simplified structure and providing an

optimal priority order for data transferring (lizuka, col. 2, ll. 61-67) to obtain the invention as specified in claims 1, 7 and 13.

Gray, Abramson and lizuka do not expressly teach the memory controller system, method and programmable logical device, comprising recording a value of a pointer

Nguyen teaches a FIFO buffer flow regulation system and method comprising wherein the control logic (Fig. 1, ref. 34) records a value of a pointer (e.g. recording the pointer value in a channel sequence registers 74-1 and 74-2 of Fig. 2) (col. 5, ll. 60 to col. 6, ll. 22), wherein the channel sequence registers comprising the input pointer (Fig. 2, ref. 86-1, 86-2) and the output pointer (Fig. 2, ref. 88-1, 88-2) for pointing to the proper slot for the next input operation and the next output operation respectively.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Nguyen's utilization of the plurality of pointers by the central control into Gray, Abramson and lizuka's control logic for the benefit of proper tracking and control regarding the accessing of the circular buffer (Nguyen, col. 5, ll. 60-66) to obtain the invention as specified in claims 1, 7 and 13.

11. As per claims 2 and 8, Gray, Abramson, lizuka and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray, Abramson and lizuka further teach the memory controller system, method and programmable logical device, comprising wherein, when returning data to the respective device from which a memory

access request requiring multiple data bursts over the memory bus was received, data is read out from a first part of the respective buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of the respective buffer (Gray, col. 12, ll. 18-30; Abramson, Fig. 5; col. 3, l. 59 to col. 5, l. 38; col. 8, l. 33 to col. 9, l. 53 and lizuka, Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57; col. 26, ll. 4-39), wherein the particular device of the plurality of devices (Gray, Fig. 3, ref. 221-224) can make request for data every other cycle, therefore data associated with the first device (Gray, Fig. 3, ref. 221) is read from the associated device buffer (Gray, device buffer 204 of Fig. 3), then data of the second device (Gray, Fig. 3, ref. 222) is read from the associated device buffer (Gray, device buffer 206 of Fig. 3), then returns to the reading the associated device buffer (Gray, device buffer 204 of Fig. 3) of the first device (Gray, Fig. 3, ref. 221).

12. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Abramson et al. (US Patent 6,499,077), lizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) as applied to claims 1 and 7 above, and further in view of Kuronuma et al. (US Patent 6,859,848).

Gray, Abramson, lizuka and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray, Abramson and lizuka further teach the memory controller system, method and programmable logical device, comprising receiving read access request is a wrapping request which require multiple memory bursts, and the control logic allocates/assigns each of said memory bursts to a respective one of said buffers

(Gray, Fig. 3, ref. 204-209; col. 5, l. 19 to col. 8, l. 63; Abramson, Fig. 5; col. 3, l. 59 to col. 5, l. 38; col. 8, l. 33 to col. 9, l. 53 and lizuka, Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57; col. 26, ll. 4-39).

Gray, Abramson, lizuka and Nguyen do not expressly teach the memory controller system, method and programmable logical device, comprising determining if the wrapping request is received.

Kuronuma teaches the controlling system and method determining if the wrapping request is received (col. 4, ll. 27-44), by combining with the above Gray, Abramson, lizuka and Nguyen's wrapping request, the wrapping request is determined by a detector detecting the number of possible sequential access to the SDRAM associated to a received DMA request, as the number of the multiple memory bursts required by the received DMA request is determined.

It would have been obvious to one of ordinary skill in this art, at the time when invention was made to include Kuronuma's detection of the number of possible sequential access of the SDRAM into Gray, Abramson, lizuka and Nguyen's control logic for the benefit of providing a relative simple configuration for accessing the memory for multiple sequential memory bursts (Kuronuma, col. 4, ll. 15-20) to obtain the invention as specified in claims 5 and 11.

13. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (US Patent 6,816,923) in view of Abramson et al. (US Patent 6,499,077),

lizuka et al. (US Patent 5,581,530) and Nguyen et al. (US Patent 5,335,326) as applied to claims 1 and 7 above, and further in view of "Microsoft Computer Dictionary".

Gray, Abramson, lizuka and Nguyen teach all the limitations of claims 1 and 7 as discussed above, where Gray, Abramson and lizuka further teach the memory controller system, method and programmable logical device, comprising wherein said memory interface is suitable for connection to/receiving data from the memory device over said memory bus in bursts (Gray, Fig. 3; col. 5, l. 19 to col. 8, l. 63; Abramson, Fig. 5; col. 3, l. 59 to col. 5, l. 38; col. 8, l. 33 to col. 9, l. 53 and lizuka, Fig. 8; Fig. 14(a) to 14(e); col. 11, ll. 5-26; col. 14, ll. 49-57; col. 26, ll. 4-39).

Gray, Abramson, lizuka and Nguyen do not expressly teach the memory controller system, method and programmable logical device, comprising a SDRAM controller, and SDRAM bursts of data.

"Microsoft Computer Dictionary" teaches the utilization of the SDRAM, wherein it is well known by one skilled in the art that SDRAM is a common type of RAM utilized within the computer system (Page 469), wherein the memory controller associated with the SDRAM would be a SDRAM controller and data transferred is SDRAM data.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Microsoft Computer Dictionary's SDRAM into Gray, Abramson, lizuka and Nguyen's memory (Gray, Fig. 3, ref. 210) for the benefit of that SDRAM can run at a higher clock speed ("Microsoft Computer Dictionary", Page 469) to obtain the invention as specified in claims 6 and 12.

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-2, 5-8 and 11-13 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 24, 2009

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181